Please cancel Claim 2, without prejudice.

In accordance with 37 CFR 1.121(c)(1)(ii), Attachment A provides marked up versions of the claims containing newly introduced changes.

REMARKS

Claim 1 was amended to incorporate the subject matter of Claim 2 and advance prosecution. Claim 2 was cancelled, without prejudice.

Claims 1-22 are pending in the above-identified application. Claims 1-17 and 19-22 are rejected under 35 U.S.C. §112, second paragraph; 35 U.S.C. §103(a); and provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-29 of copending Application No. 09/204,585 in view of DeWard (U.S. 4,155,119). The rejections are respectfully traversed in light of the following remarks, and reconsideration is requested.

A telephonic interview was held on March 2, 2001, between the Examiner and Matthew Spark and Ken Koestner. During the interview, with respect to the rejection of Claim 1, the Examiner repeatedly stated that he did not believe the description of the decoder disclosed "how the decoder is doing what it is doing" and that the "decoder is for decoding instructions". The Examiner insisted that engineering circuitry diagrams were required to prove to his satisfaction that the decoder performed the functions described in the specification. Mssrs. Spark and Koestner discussed that the specification accurately described the decoder, its functions and that one of ordinary skill in the art would be aware of methods, such as Verilog, to translate function into structure. The Examiner failed to assert any reference, case law or MPEP section to support his position that the decoder was not capable

of performing the described function.

Claims 1-17 & 19-22 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In the rejection, the Examiner stated:

> Details of the rejections have already been set forth in the last Office Action. The details are incorporated by reference thereto.
>
> With respect to the remarks directed to claim 1, it is not seen how the last two lines of claim 1 are related to the function unit and the register file because the functional unit and the register file as recited are not involved in implicitly deriving specifier based on another.
>
> With respect to the remarks directed to the decoder, a decoder is commonly used for decoding instructions, as disclosed in lines 16-19 of page 18 of the specification and not for implicitly deriving specifiers.as recited in the claims. There is no explanation in the specification as to how the empty rectangular boxes representing a prior art decoder as shown in Figure 6 is able to implicitly derive specifiers.
>
> With respect to the remarks directed to claim 19, applicants allege that the disclosure in lines 16-19 of page 8 of the specification supports the claim language. The identified excerpt merely discloses that the decoder decodes instructions. Apllicants [sic] fial [sic] to explain how the excerpt support the functional language

In response to the rejection of Claim 1, Applicants respectfully contend that the last two lines of claim 1 are related to the register file and the function unit. The last two lines describe the instruction which "operat[es] upon a plurality of registers in the register file." (Claim 1, line 4) The instruction is executed in the functional unit. The instruction is described as one "in which a register specifier is implicitly derived, based on another register specifier" (i.e., the register specifier operating upon the plurality of registers in the register file is implicitly derived from another register specifier). As Claims 5-16 are dependent upon Claim 1, the relationship between the last two lines of Claim 1 and the register file and functional unit is the same as in Claim 1.

In response to the rejection, Applicants respectfully contend that the function of the

decoder is clear and based on the specification. Examiner stated in an earlier Office Action:

> It is not seen how a decoder which is for decoding instructions to generate control signals is able to derive implicit register from explicit register specifier.

Claim 2 claims:

> a decoder coupled to the functional unit and coupled to the register file, the decoder implicitly deriving a register specifier based on an explicitly-specified register specifier of the instruction.

Claim 17 claims:

> a decoder coupled to the functional unit and coupled to the register file, the decoder implicitly deriving a register specifier based on an explicitly-specified register specifier of the instruction and generating a first pointer to the explicitly-specified register and a second pointer to the implicitly-derived register.

On page 18, lines 16-19 of the specification, one technique for implicitly deriving a register specifier is clearly stated:

> the decoder **602** decodes instructions that use implicitly-derived register specifiers and reads the explicitly-defined register. The decoder **602** then generates pointers both to the explicitly-defined register and to the implicitly-derived register.

The language of the claims is clearly supported by the Specification. While limitations in the specification are not to be read into the claims, claims are interpreted in light of the specification.

In response to the rejection of Claim 19, Applicants respectfully contend that the function of the register file is clear and based on the specification. Examiner stated in an earlier Office Action that the:

> function of the register file is not clear. It is not seen how a register file which is commonly having a plurality of registers for storing data is able to generate two pointers as recited. Further, claim 19 fails to recite how the function unit and the register file of parent claim uses the pointers so that meaningful operation can be achieved.

Claim 19 claims:

> a pointer coupled to the register file and designating a register in the register file, the pointer including a signal indicative of selection of a implicitly-derived register, the register file generating two pointers, one directed to the explicitly-specified register and a second directed to the implicitly-derived register when implicit derivation of a register specifier is selected.

On page 18, lines 16-19 of the specification, one technique for implicitly deriving a register specifier is clearly stated:

> a pointer to registers within the register file segments **610**, **612**, **614**, and **616** includes an additional bit indicating that a register read is accompanied by a read of an implicitly-derived register.

The language of the claims is clearly supported by the Specification. While limitations in the specification are not to be read into the claims, claims are interpreted in light of the specification.

In response to the rejection of Claims 1-22, Applicants respectfully contend that it is clear what is meant by "explicitly define" and "implicitly derive". The Examiner stated that:

> it is not clear what is meant by "explicitly define" and "implicitly derive" are.

The Doubleday Dictionary (First Edition, 1975) defines "explicit" as:

> 1: Plainly stated; clearly expressed. 2: Having no disguised meaning or reservation; definite; open.

It is clear from the plain meaning of the term that something that is "explicitly defined" is one that is clearly expressed. The explicitly defined register specifier is one that is given.

The Doubleday Dictionary (First Edition, 1975) defines "implicit" as

> 1: Implied or to be understood, but not specifically stated. 2: Absolute; unquestioning. 3: Virtually contained or involved in, though not immediately apparent or stated; inherent.

It is clear from the plain meaning of the term that something, such as a value, that is "implicitly derived" from something else, such as another value, is implicitly derived because there is a relationship between the two values. There is a relationship between the implicitly derived register specifier and the explicitly defined register specifier.

Therefore, for the above reasons, Applicant respectfully requests reconsideration and withdrawal of the rejections of Claims 1-22 under 35 U.S.C. § 112, second paragraph.

Claims 1-22 were rejected under 35 U.S.C. §103(a) as being unpatentable over Fleck (US 6,067,159) in view of DeWard (US 4,155,119). In the rejection, the Examiner stated:

> In the remarks directed to the prior art rejections, applicants admit that Fleck discloses a processor having a register file, a decoder and an execution unit. However, applicants contend that there is no memtion [sic] in Fleck that the processor that the processor executes an instruction set having instructions in which register is implicitly derived based on another register file. Note that the claims do not recite any circuits for implicitly derive specifiers. If the the [sic] function unit , the decoder and the register file as recited in the claims are able to process an instruction having a register specifier regardless of whether they are implicitly, explicitly, defined or derived, so do the processor of Fleck.

In response, Applicants contend that the obviousness rejection under 35 U.S.C. § 103 cannot be established by combining the teachings of Fleck and DeWard because there is no suggestion or motivation in the cited references for combining Fleck and DeWard.

The Examiner partly bases his rejection of the claims upon the unique proposition that any function performed by a structure in the claims is capable of being performed by an equivalent structure in a reference even if the reference does not disclose that function. The Examiner failed to assert any case law or MPEP section to support this unique theory. In fact, the Examiner's theory is nothing more than impermissible hindsight. An Examiner can not reject a claim upon the basis that a similar structure in a reference is capable of performing a

function not disclosed or contemplated in that reference.

Additionally, the Examiner fails to provide any support to combine references. "For a proper obviousness combination, the prior art references must provide a suggestion or motivation to make such a combination." Heidelberger Druckmaschinen AG v. Hantscho Commercial Prods., Incs., 21 F.3d 168, 1072, 30 USPQ2d 1377, 1379 (Fed. Cir. 1994) *citing* Northern Telecom Inc. v. Datapoint Corp., 908 F.2d 931, 934 15 USPQ2d 1321, 1323 (Fed. Cir. 1990). The Examiner misconstrues what is required to combine references for a prima facie case of obviousness. In Ruiz v A.B. Chance Co., 234 F.3d 654 (Fed. Cir. 2000), the Court specifically held *specific findings must be made establishing why it was "apparent" to use a feature of found in one reference in the context with what is disclosed in another reference.* (The district court must make specific findings establishing why it was "apparent" to use the screw anchor of the Fuller and Rupiper method in combination with the metal bracket as used in the Gregory patents.).

While the references need not expressly teach that the disclosure contained therein should be combined with another, see Motorola, Inc. v. Interdigital Tech. Corp., 121 F.3d 1461, 1472, 43 USPQ2d 1481, 1489 (Fed. Cir. 1997), the showing of combinability must be "clear and particular." In re Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617. [Emphasis added]. The Examiner has *utterly failed* to make any showing of combinability that is "clear and particular".

Fleck discloses a data register file 300 (col. 4, line 22)., a decoder 11a (col. 3, lines 3); and an execution unit 11b (Fleck, col. 3, line 4). More particularly, Fleck discloses a data processor comprising a first pipeline for decoding and executing data instructions, a second pipeline for decoding and executing address instructions, a unit for issuing multiple instructions to the pipelines, a first set of registers coupled with the first pipeline and a second set of registers coupled to the second pipeline where the first and second pipelines process

data in parallel. (Fleck, Abstract). However, there is no mention that the processor executes an instruction set including instructions in which a register specifier is implicitly derived, based on another register specifier, as is being claimed by Applicant. Furthermore, Fleck teaches a different processing method from Applicant in that Fleck teaches the elimination of precautions. (Fleck, col. 1, lines 59-62). Therefore, Fleck is directed to solving the problem of a processor with the capability of fast execution without the necessity of taking a number of precautions, such as dependency checks, completion analysis, resource checks, reservation stations and reorder buffers (Fleck, col. 1, lines 33-35, 50-51, 59-62). Thus, Fleck reduces the precautions taken during parallel processing (Fleck, col. 1, lines 59-62) while Applicant uses a technique and processor architecture enhancement that improves the efficiency of instruction coding and reduces the bit resource allocation within an instruction word that is dedicated to register specification (Specification, page 3, lines 15-17). Rather than eliminating precautions, Applicant improves the efficiency of instruction coding and reduces the bit resource allocation within an instruction word that is dedicated to register specification

Fleck does not teach the use of a processor executes an instruction set including instructions in which a register specifier is implicitly derived, based on another register specifier. In fact, Fleck seems to be used by the Examiner merely to supply the structures while DeWard seems to be used merely to show that the claimed functionality is old. Even if Fleck and DeWard were combined, the claimed invention would not be the result.

While the invention disclosed in DeWard relates generally to input/output operations in a digital computer and specifically to a method of addressing memory for input/output operations in a digital computer (DeWard, col. 1, lines 6-10), DeWard is directed to addressing a completely different problem than Fleck. Fleck was addressed to solving the problem of a processor with the capability of fast execution without the necessity of taking a number of precautions, such as dependency checks, completion analysis, resource checks,

reservation stations and reorder buffers (Fleck, col. 1, lines 33-35, 50-51, 59-62). DeWard, on the other hand, discloses a method for converting virtual addresses into real addresses utilizing a page table which were intended to apply virtual addressing techniques to the input/output section of the digital computer which such techniques had previously been confined to memory access involving the central processing unit of the digital computer (DeWard, col. 1, line 42 to col. 3, line 21). There is no suggestion in Fleck that a processor executing an instruction set including instructions in which a register specifier is implicitly derived, based on another register specifier, is desirable nor does DeWard suggest a combination of its virtual addressing technique with the precaution reduction technique of Fleck.

DeWard is different from the claimed invention in a number of ways. For example, DeWard relates to a memory management operation by a digital computer and the claimed system relates to decoding of an instruction including determining the instruction operation, and determining the operands that are operated upon by the instruction.

DeWard relates to memory management, i.e., the addressing of memory distributed throughout multiple devices connected to a single input/output channel, while the claimed system related to specification of registers in a register file. Memory management is irrelevant to specification of registers for an instruction.

DeWard describes a memory management operation for treating the externally specified address coming from one of multiple devices external to the digital computer. (See DeWard, Abstract) The claimed system, on the other hand, relates to a decoding operation that determines the registers to be operated upon by the decoded instruction.

DeWard relates to memory management operations that are external to a processor. The claimed system relates to the fundamental operations of decoding and defining the instruction and instruction operations that are performed within a processor.

DeWard solves the problem of addressing memory in a large instruction space while the claimed system supports efficient coding of an instruction for execution by a processor.

Obviousness is tested by "what the combined teachings of the references would have suggested to those of ordinary skill in the art." In re Keller, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). But obviousness "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." ACS Hosp. Sys. Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). Thus, "teachings of references can be combined only if there is some suggestion or incentive to do so." Id. Applicants, thereby, contend that there is no suggestion or incentive to combine Fleck and DeWard because Fleck and DeWard are directed to solving different with different solutions, as outlined above.

Thus, for a obviousness combination, the "critical inquiry is whether 'there is something in the prior art as a whole to suggest the desirability, and thus the obviousness of making the combination.'" Fromson v. Advance Offset Place, Inc., 755 F.2d 1549, 1556, 225 USPQ 26, 31 (Fed. Cir. 1985) *quoting* Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co., 730 F.2d 1453, 1452, 221 USPQ 481, 488 (Fed. Cir. 1984). In other words, the "mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification." In re Gordon, 773 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984) *citing* Carl Schenck, A.G. v. Nortron Corp., 713 F.2d 782, 787, 218 USPQ 698, 702 (Fed. Cir. 1983). Fleck does not suggest the desirability of a combination with DeWard because, as mentioned above, Fleck and DeWard are directed toward different problems with different solutions. Accordingly, Fleck does not suggest to one skilled in the art the desirability to search for other ways that improve the efficiency of instruction coding and reduce the bit resource allocation within an

instruction word that is dedicated to register specification, much less for a combination with a reference having a different problem and different solution, such as DeWard.

Furthermore, the "statute, §103, requires much more, i.e., that it would have been obvious to produce the claimed invention at the time it was made without the benefit of hindsight." Orthokinetics, Inc. v. Safety Travel, Chairs, Inc., 806 F.2d 1565, 1575, 1 USPQ2d 1081, 1087 (Fed. Cir. 1986). "When prior art references require selective combination by the court to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gleaned from the invention itself." Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985) *citing* ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577 & n.14, 221 USPQ 929, 933 & n.14 (Fed. Cir. 1984). Applicants believe the motivation to combine Fleck with DeWard is derived from Applicants' invention since there is no suggestion in the cited references for the desirability of such a combination.

Examiner's 103 rejection of Claims 1-22 was also procedurally inadequate as the rejection failed to provide any basis for combining Fleck and DeWard and also failed to show that the combined prior art references teach or suggest *all claim limitations*. The Examiner merely stated that:

> Fleck discloses a processor having a register file 300, a decoder and an execution unit (11a and 11b). Fleck does not state how addresses of the register file (a memory) are formulated. However, DeWard teaches in Figure 7 that an address (218) (read on explicit address) of a memory can be generated by concatenating a page number (from table 215) to a displacement (210). The next address (read on implicit address derived from the explicit address) can be derived from the previous address by merely incrementing the displacement with an offset value. If the memory management of DeWard is implemented in the register file of the Fleck system, it would have been obvious to a person of ordinary skill in the art to generate register address as taught by DeWard so that the register file in Fleck can be accessed.

With all due respect, the Examiner failed to provide any explanation as to what was the suggestion or motivation in the references rendering it obvious to use the memory management of DeWard in the register file of Fleck. Additionally, the Examiner's rejections appeared to only address independent claims 1 & 20 and failed address the features of dependent claims 2-19, 21 & 22. MPEP 706.02(j) [Contents of a 35 USC 103 Rejection] clearly spells out the criteria an Examiner must meet in order to issue a rejection under 35 USC 103:

> 35 USC 103 authorizes a rejection where, to meet the claim, it is necessary to modify a single reference or to combine it with one or more other references. After indicating that the rejection is under 35 USC 103, the examiner should set forth in the Office action:
>
> (A) the relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate,
>
> (B) the difference or differences in the claim over the applied reference(s),
>
> (C) the proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and
>
> (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification.
>
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, *there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.* Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest *all claim limitations*. The teaching or suggestion to make the claimed combination and reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP 2143-2143.03 for decisions pertinent to each of these criteria.
>
> *The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done.* "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why

> the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." *Ex parte Capp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). See MPEP 2144-2144.09 for examples of reasoning supporting obviousness rejections.
>
> Where a reference is relied on to support a rejection, whether or not in a minor capacity, that reference should be positively included in the statement of rejection. See *In re Hoch*, 428 F.2d 1341, 1342 n.3 166 USPQ 406, 407 n.3 (CCPA 1970).
>
> *It is important for an examiner to properly communicate the basis of a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply.* Furthermore, if an initially rejected application issues as a patent, the rationale behind an earlier rejection may be important in interpreting the scope of the patent claims. Since issued patents are presumed valid (35 USC 282) and constitute a property right (35 USC 261), the written record must be clear as to the basis for the grant. Since patent examiners cannot normally be compelled to testify in legal proceedings regarding their mental processes (See MPEP 1701.01), it is important that the written record clearly explain the rationale for decisions made during prosecution of the application. [emphasis added]

Therefore, because Applicants contend that the combination of Fleck and DeWard was both substantively and procedurally improper, Applicants respectfully request reconsideration and withdrawal of the rejections to Claims 1-22 under 35 U.S.C. § 103(a).

Claims 1-22 were provisionally rejected under the judicially created doctrine of double patenting over claim 1-29 of copending Application No. 09/204,585 in view of DeWard (U.S. 4,155,119). In the rejection, the Examiner stated:

> The claims of 09/204,585 recites a plurality of functional units and a register. The claims do not state how addresses of the register file (a memory) are formulated. However, DeWard teaches in Figure 7 that an address (218) (read on explicit address) of a memory can be generated by concatenating a page number (from table 215) to a displacement (210). The next address (read on implicit address derived from the explicit address) can be derived from the previous address by merely incrementing the displacement with an offset value. If the memory management of DeWard is implemented in the register file of 09/204,585, it would have been obvious to a person of ordinary skill in the art to generate register address as

taught by DeWard so that the register file can be accessed.

This is a provisional obviousness-type double patenting rejection.

In response, Applicants recognize the provisional nature of the rejections, and will address the substantive aspect of this issue in future communications to this Office should Claims 1-29 of copending Application No. 09/204,585 be allowed at some future point in time and in the same, or substantially the same, form as they now presently exist.

CONCLUSION

For the foregoing reasons, Applicant believes the pending Claims 1, 3-17, 19-22 are allowable, and a Notice of Allowance is respectfully requested. The Examiner is invited to call the Applicants' Attorney at (949) 718-6780 for any questions with this response.

EXPRESS MAIL LABEL NO:

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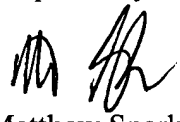
Respectfully submitted,



Matthew Spark
Attorney for Applicant(s)
Reg. No. 43,453

ATTACHMENT A

IN THE CLAIMS

This response amends claim 1 as follows:

1. A processor comprising:

a register file including a plurality of registers; [and]

a functional unit coupled to the register file, the functional unit that executes an instruction operating upon a plurality of registers in the register file, the instruction in which a register specifier is implicitly derived, based on another register specifier[.] ;

a decoder coupled to the functional unit and coupled to the register file, the decoder implicitly deriving a register specifier based on an explicitly-specified register specifier of the instruction.